REMARKS/ARGUMENTS

Applicant affirms the election of claims 76 - 106.

Claims 101 and 107 - 134 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Applicants reserve the right to file one or more divisional applications.

Claims 76 - 80, 82, 85 - 96, 99, 105 and 106 have been amended.

Claims 76 - 100 and 102 - 106 are pending in the application.

With regard to the specification, it is requested that the Examiner disregard the amendments made to the specification in the amendment filed October 21, 2004. In amending the specification, a copy of the PCT application was inadvertently used to request the amendments to the specification and therefore resulting in incorrect page and line numbers. These line and page numbers have been corrected in the present amendment. There have been no changes made to the amendatory material, it being identical to the amendment filed on October 21, 2004. The undersigned attorney is sorry for any inconvenience this may have caused the Examiner.

Applicants' undersigned counsel appreciates the Examiner's comments regarding the language: "and does not contain any said shift clock pulse during a capture operation," and has deleted same from the claims, thereby obviating the 35 U.S.C. §112, first and second paragraph rejections.

As a further result, applicant has defined shift clock pulse "in scan mode" and capture clock pulse "in normal mode". This is

to clarify the Examiner's concern that a capture clock should contain only capture clock pulses, and a shift clock should contain only shift clock pulses.

In many designs, a clock domain may be only controlled by one test clock. Thus, this test clock will contain clock pulses applied in scan mode (hence shift clock pulses) and clock pulses in normal mode (hence capture clock pulses).

Applicant happened to call the test clock "the capture clock", which inadvertently and unfortunately has created some confusion.

The rejection of the basic claims 76 - 79, 81, 85 - 95, 102, 105 and 106 under 35 U.S.C. §103 as being obvious in view of Nadeau-Dostie1 and Nadeau-Dostie2 is respectfully traversed for the following reasons:

In Nadeau-Dostie1 and Nadeau-Dostie2, the domain clocks are mainly used for testing delay faults within a clock domain. To test a delay fault, it is required to apply "two consecutive domain clock pulses" at the domain's rated clock speed.

Nadeau-Dostie1 (see Fig. 4) teaches to launch the first domain clock pulse (Launch HS in Fig. 4) using the last bit of the test stimuli "in scan mode" (when ScanEnableHS=1) and the second domain clock pulse (Capture in Fig. 4) to perform the capture operation "in normal mode" (when ScanEnableHS=0). The delay test approach is called skewed-load using "a shift followed by a capture" pulses. Same approach was also used in Nadeau-Dostie2 (see FIG. 4). A1 is

launched "in scan mode", when MS1=1, and B1 is launched "in normal mode", when MS1=0.

Same theory applies to A2 and B2, and A3 and B3.

In the present application, both domain clock pulses are launched "in normal mode". The delay test approach is called broadside using double-capture comprising "a capture followed by a capture" pulses.

Although Nadeau-Dostie2 teaches an ordered sequence of clock signals for testing delay faults, the first domain clock pulse must be launched in "scan mode", while in the present application, the first domain clock pulse is launched in "normal mode".

Also, "all" second domain clock pulses (see B1, B2, and B3 in FIG. 4) in Nadeau-Dostie2 must be aligned at the same positive edge so that they can be "all" captured simultaneously, which leads to power consumption problems since all scan cells would be triggered simultaneously every few cycles. In contrast, the present application, however, "all" second domain clock pulses can be placed in a staggered order or in a sequential order.

This will acknowledge the interview courteously granted to applicants' undersigned attorney, the inventor Laung-Terng Wang and his associate Shianling Wu on March 31, 2005. At the interview, Dr. Wang explained the basic fundamental difference between the timing waveforms that are set out in claims 76 and the timing waveform of Nadeau-Dostie2 using the attached wave form diagram. Dr. Wang showed and explained how the language of claim 76 reading:

> (b) applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response;...

was not shown, taught or suggested by the art and the resulting nonobvious advantages thereof which includes the asynchronous clock domains.

It was also noted that not only does the present invention eliminate clock skew problems (see col.7, lines 65-67 in Nadeau-Dostie2) that would have otherwise used two-edge or two-phase clocking scheme (see col.8, lines 7-28 in Nadeau-Dostie2), it can also ease IC layout problems, because now MS1, MS2, and MS3 (see FIG.4 of Nadeau-Dostie2) do not need to operate at their respective domain clock rates, but at a common slow speed. Most importantly, the present invention can allow testing of asynchronous clock domains, e.g., CK1=100MHz, CK2=77MHz, and CK3=53MHz, unlike Nadeau-Dostie2 (see FIG. 4), CK1=100MHz, CK2=50MHz, and CK3=25MHz, for instance.

The rejection of claims 80, 82-84, 96-101, 103 and 104 on various combinations of Nadeau-Dostie1 and Nadeau-Dostie2 with Nadeau-Dostie3 and/or Rajski (US 5,991,909) or Benoit et al (US 6,442,722) are clearly avoided for the reasons given above.

In view of the above, further and favorable reconsideration is respectfully requested.

A Request for Continued Examination (RCE) Transmittal is being filed concurrently herewith.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Applicants

Attachments: Request for Continued Examination (RCE) Transmittal
Waveform diagram

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: April 5, 2005

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.